Final Exam Report

**1. Draw a 1-bit full adder (FA), 2-input NAND, and 2-input AND cells using MAGIC, make sure it passes all DRCs, extract the circuit level netlist, and simulate its behaviour using SPICE. (2 points each: 6 points total)**

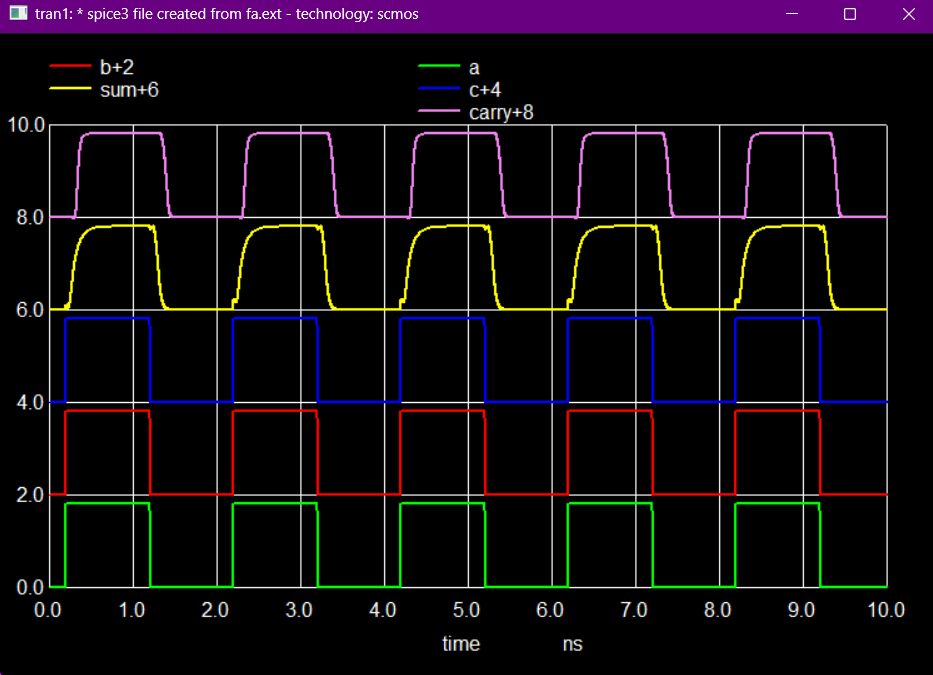
**Full Adder:**

A computer screen shot of a diagram

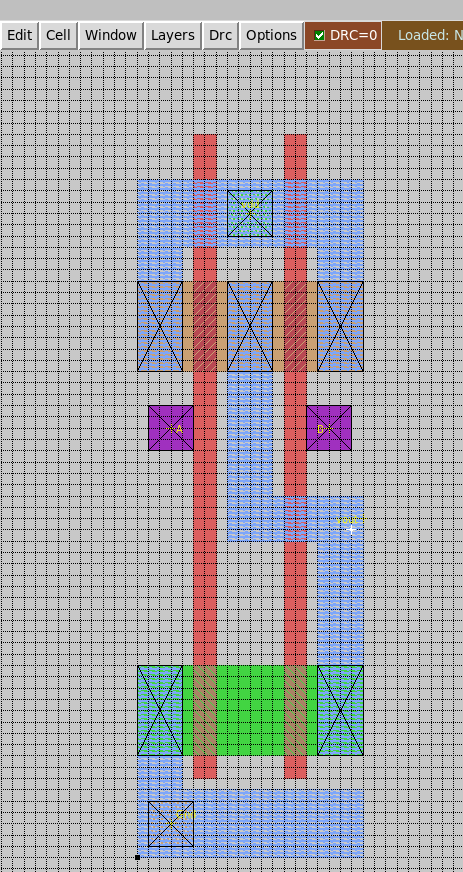
Description automatically generated

The NGspice results for inputs:

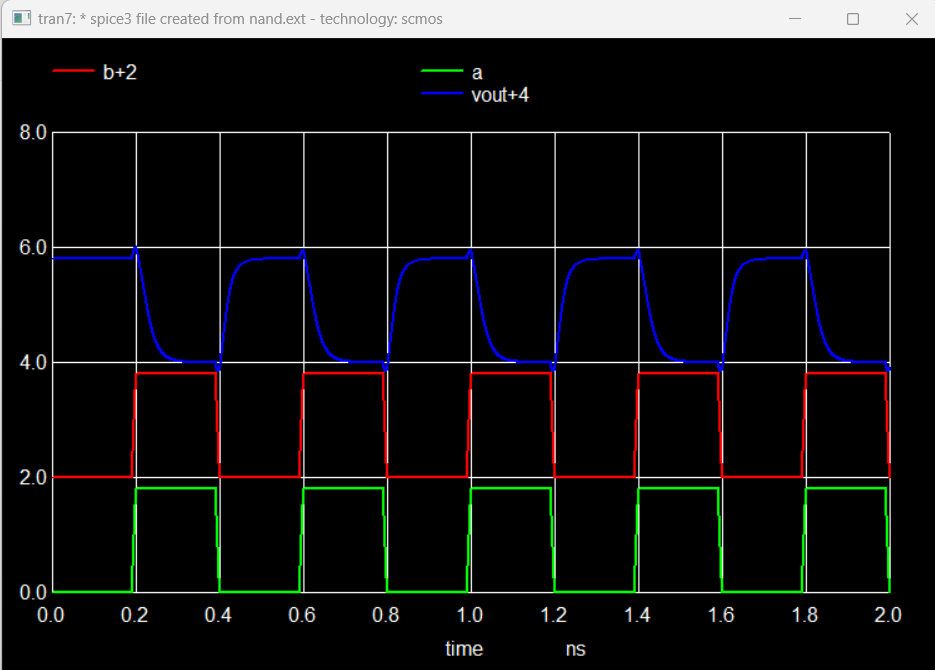
1. A=1, B=1, cin=1 result: Sum= 1 , cout=1



**Nand Gate:**



A=1 B=1



**And Gate:**

A grid with many squares

Description automatically generated with medium confidence

A=1 B=1

A screen shot of a graph

Description automatically generated

**2. Use hierarchical design flow to instantiate cells from Q1 to create CSA-W (white) and CSA-G (grey) cells shown on slide-3, make sure it passes all DRCs, extract the circuit level netlist, and simulate their behaviour using SPICE. (2 points each: 4 points total)**

**CSA-White:**

A computer generated image of a network

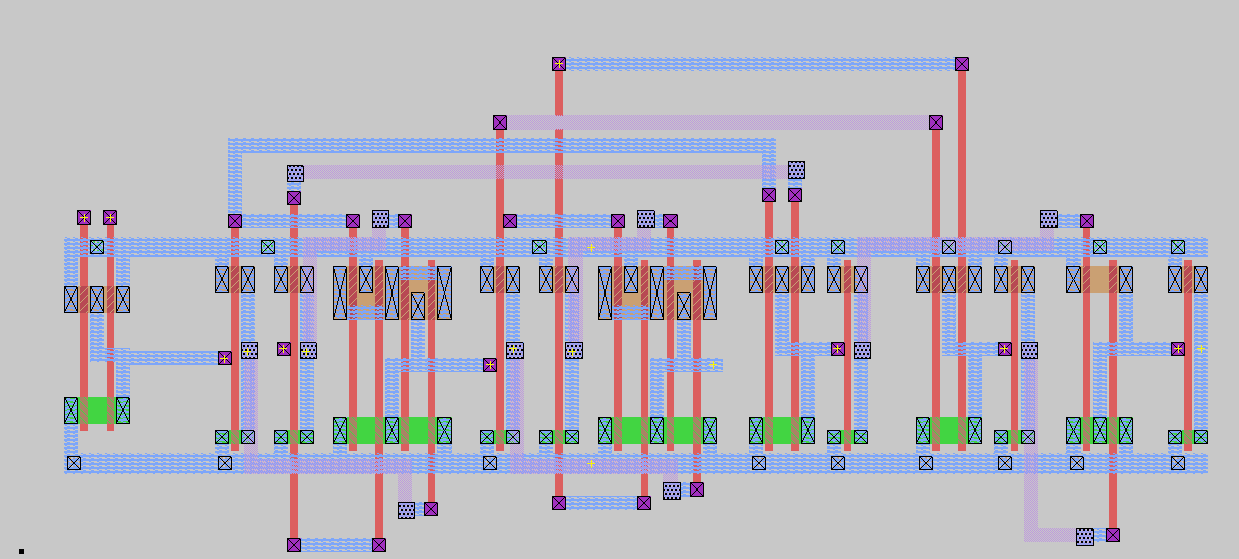
Description automatically generated with medium confidence

X-1 Y-1 And gate Output is high, so A=1 B=1 C=1 sum=1 Carry=1

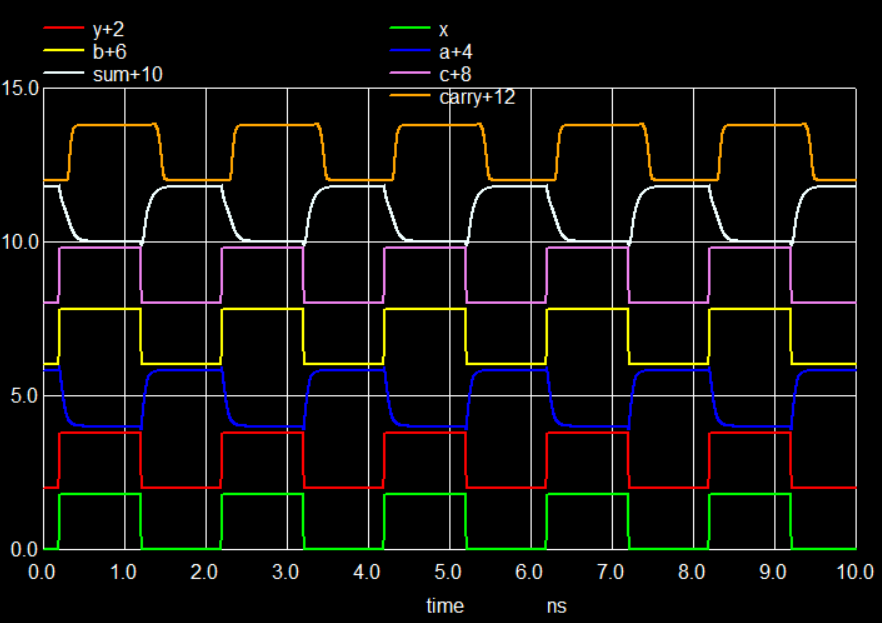
A graph with colorful lines

Description automatically generated

**CSA- Grey:**



X-1 Y-1 Nand gate Output is low, so A=0 B=1 C=1 sum=0 Carry=1



**3Q) Use hierarchical design flow to instantiate CSA-W (white), CSA-G (grey), and FA cells from Q2 and flip-flops from DE-5, to create a 2-bit Baugh-Wooley signed multiplier shown on slide-4. Make sure it passes all DRCs, extract the circuit level netlist. (10 points)**

The top and right rail is VDD and bottom and left rail is Gnd

A computer screen shot of a diagram

Description automatically generated

Here the row left FA input A is connected to VDD.

A diagram of a block diagram

Description automatically generated

Case1: 0 x 0 = 0000

X1, X0= 0 0

Y1, Y0= 0 0

S3, S2, S1, S0= 0 0 0 0 ( in the plot Sum3 is always high because A is connected to Vdd)

A screen shot of a graph

Description automatically generated

Case2: 1 x 1=1(decimal)

X1, X0= 0 1

Y1, Y0= 0 1

S3, S2, S1, S0= 0 0 0 1 ( S0 is white in colour) at t=3ns

A graph with colorful lines

Description automatically generated

Case3: 1 x -1= 0011( -1 in decimal)

X1, X0= 0 1

Y1, Y0= 1 1(-1 in decimal)

S3, S2, S1, S0= 0 0 1 1(-1 in decimal) (S0-white in colour and S1-orange) at t=3ns

A graph with colorful lines

Description automatically generated

Case4: -2 x -1= 0010( 2 in decimal)

X1, X0= 1 0 (-2 in decimal)

Y1, Y0= 1 1(-1 in decimal)

S3, S2, S1, S0= 0 0 1 0( 2 in decimal) ( S1-orange) at t=3ns

A screen shot of a graph

Description automatically generated

**Q5) Find the maximum clock frequency using SPICE. (2 points).**

**A diagram of a diagram

Description automatically generated**

The Critical path is marked with a dotted line where, the delay is from two CSA-G’s and two FA’s.

The max clock frequency is 0.24 Ghz.

A screenshot of a computer code

Description automatically generated